WHAT IS CLAIMED IS:

1. A contact structure of a semiconductor device, the contact structure comprising:

a dry-etchable lower conductive film;

an upper conductive film formed on the lower film and including Al or Al alloy, the upper film having edges located on the lower film;

an insulator having a contact hole exposing at least a portion of the lower film; and

an IZO layer formed on the insulator and contacting the lower film through the contact hole.

2. The contact structure of claim 1, wherein the contact hole exposes at least one edge of the lower film.

3. The contact structure of claim 1, wherein the distance between the edges of the lower film and the edges of the upper film is substantially uniform.

4. The contact structure of claim 1, wherein the lower film comprises Cr.

5. A method of forming a contact structure of a semiconductor device, the method comprising:

forming a lower conductive film;

forming an upper conductive film on the lower film, the upper film including Al or Al alloy;

forming a photoresist on the upper film;

wet-etching the upper film using the photoresist as an etch mask to produce undercut under the photoresist;

dry-etching the lower film using the photoresist as an etch mask;

forming an insulating layer having a contact hole exposing at least a portion of the lower film; and

forming an IZO layer on the insulating layer, the IZO layer contacting the lower film through the contact hole.

6. The method of claim 5, wherein the contact hole exposes at least one edge of the lower film.

7. The method of claim 5, wherein the lower film comprises Cr.

8. A thin film transistor array panel comprising:

a gate conductive layer formed on an insulating substrate;

a gate insulating layer on the gate conductive layer;

a semiconductor layer on the gate insulating layer;

a data conductive layer formed at least in part on the semiconductor layer;

a passivation layer formed on the data conductive layer; and

an IZO conductive layer formed on the passivation layer,

wherein at least one of the gate conductive layer and the data conductive layer includes a dry-etchable lower film and an upper film formed on the lower film, the upper film including Al or Al alloy and having edges located on the lower film, and the IZO conductive layer contacts the lower film.

9. The thin film transistor array panel of claim 8, wherein edges of the lower film are located near edges of the upper film adjacent thereto.

10. The thin film transistor array panel of claim 8, wherein the IZO conductive layer contacts an edge of the lower film.

11. The thin film transistor array panel of claim 8, wherein the IZO conductive layer contacts the upper film.

12. The thin film transistor array panel of claim 8, wherein the distance between edges of the lower film and edges of the upper film adjacent thereto is substantially uniform.

13. The thin film transistor array panel of claim 8, wherein the lower film comprises Cr.

14. The thin film transistor array panel of claim 13, wherein the lower film has a thickness equal to or less than about 500 Å.

15. The thin film transistor array panel of claim 8, wherein the data conductive layer comprises a data line and a drain electrode separated from each other, and the IZO conductive layer comprises a pixel electrode contacting the drain electrode, a gate contact assistant contacting a portion of the gate conductive layer, and a data contact assistant contacting a portion of the data line.

16. The thin film transistor array panel of claim 15, wherein the semiconductor layer has substantially the same planar shape as the data conductive layer except for a portion located between the data line and the drain electrode.

17. The thin film transistor array panel of claim 8, wherein the passivation layer contacts the semiconductor layer.

18. A method of manufacturing a thin film transistor array panel, the method comprising:

forming a gate conductive layer on an insulating substrate;

forming a gate insulating layer;

forming a semiconductor layer;

forming a data conductive layer including a data line and a drain electrode;

forming a protective layer having a contact hole on at least a portion of the gate conductive layer and the data conductive layer; and

forming an IZO conductive layer connected to at least a portion of the gate conductive layer and the data conductive layer through the contact hole,

wherein the at least a portion of the gate conductive layer and the data conductive layer includes a dry-etchable lower film and an upper film made of Al or Al alloy.

19. The method of claim 18, wherein the formation of the at least a portion of the gate conductive layer and the data conductive layer comprises:

sequentially depositing the lower film and the upper film;

forming a photoresist on the upper film;

wet-etching the upper film; and

dry-etching the lower film.

20. The method of claim 19, wherein the lower film comprises Cr.

21. The method of claim 20, wherein the lower film has a thickness equal to or less than about 500 Å.

22. The method of claim 18, wherein the semiconductor layer comprises an intrinsic film and an extrinsic film.

23. The method of claim 22, wherein the formation of the data conductive layer and the semiconductor layer is performed by etching with a single photoresist, and the photoresist comprises a first portion with a first thickness located on a wire area, a second portion with a second thickness smaller than the first thickness located on a channel area, and a third portion thinner than the second portion and located on a remaining area.

24. The method of claim 23, wherein the photoresist is formed by using a single mask.

25. The method of claim 24, wherein the formation of the gate insulating layer, the intrinsic film, the extrinsic film, and the data conductive layer comprises:

sequentially depositing the gate insulating layer, an intrinsic amorphous silicon film, an extrinsic amorphous silicon film, a lower film and a upper film, which include first portions on the wire area, second portions on the channel area, and third portions on the remaining area;

coating a photoresist on the conductor layer;

exposing the photoresist to light through a mask;

developing the photoresist;

forming the data conductive layer, the extrinsic film, and the intrinsic film by removing the third portions of the upper film, the lower film, the extrinsic amorphous silicon film, and the intrinsic amorphous silicon film, and the second portions of the upper film, the lower film and the extrinsic amorphous silicon film; and

removing the photoresist pattern.

26. The method of claim 24, wherein the formation of the data conductive layer, the extrinsic film, and the intrinsic film comprises:

performing wet etching to remove the third portion of the upper film and to expose the third portion of the lower film;

performing dry etching to remove the third portion of the lower film and to expose the third portion of the extrinsic amorphous silicon film;

performing dry etching to remove the third portions of the extrinsic amorphous silicon film and the intrinsic amorphous silicon film and the second portion of the photoresist such that the second portion of the upper film is exposed and the intrinsic film is completed from the intrinsic amorphous silicon film;

removing the second portion of the upper film;

removing the second portion of the lower film such that the data conductive layer is completed;

removing the second portion of the extrinsic amorphous silicon film such that the extrinsic film is completed; and

removing the first portion of the photoresist.

27. The method of claim 26, wherein the removal of the first portion of the photoresist is performed between the removal of the second portion of the upper film and the removal of the second portion of the lower film.

28. A thin film transistor array panel comprising:

a gate line formed on an insulating substrate;

a gate insulating layer on the gate line;

a semiconductor layer on the gate insulating layer;

a data line formed at least in part on the semiconductor layer;

a drain electrode formed at least in part on the semiconductor layer and spaced apart from the data line;

a passivation layer formed on the semiconductor layer and having a first contact hole exposing the drain electrode, a second contact hole exposing a portion of the gate line, and a third contact hole exposing a portion of the data line;

a pixel electrode connected to the drain electrode through the first contact hole;

a gate contact assistant connected to the gate line through the second contact hole; and

a data contact assistant connected to the data line through the third contact hole and having unevenness.

29. The thin film transistor array panel of claim 28, wherein the data line comprises a Cr film and an Al film on the Cr film.

30. The thin film transistor array panel of claim 29, wherein the data contact assistant comprises IZO.

31. The thin film transistor array panel of claim 28, further comprising an ohmic contact layer interposed between the semiconductor layer and the data line and the drain electrode and having substantially the same planar shape as the data line and the drain electrode, and the semiconductor layer has substantially the same planar shape as the ohmic contact layer except for a portion located between the data line and the drain electrode.

32. A thin film transistor array panel comprising:

an insulating substrate;

a gate electrode formed on the substrate;

a gate insulating layer on the gate electrode;

a semiconductor layer on the gate insulating layer opposite the gate electrode;

a data line formed at least in part on the semiconductor layer and having a trench;

a drain electrode formed at least in part on the semiconductor layer and spaced apart from the data line;

a passivation layer formed on the semiconductor layer and having a first contact hole exposing the drain electrode and a second contact hole exposing the trench of the data line;

a pixel electrode connected to the drain electrode through the first contact hole; and

a data contact assistant connected to the data line through the second contact hole and extending along the trench of the data line.

33. The thin film transistor array panel of claim 32, wherein the data line comprises a Cr film and an Al film on the Cr film.

34. The thin film transistor array panel of claim 33, wherein the data contact assistant comprises IZO.

35. The thin film transistor array panel of claim 33, wherein the trench is provided at the Al film.

36. The thin film transistor array panel of claim 32, wherein the trench exposes the substrate.